

## HIGH SPEED INTERFACE TYPE DEVICE

### ABSTRACT OF THE DISCLOSURE

5           A high speed interface type device can reduce power consumption and  
a circuit area, and transmit/receive a 4 bit data in one clock period. The high  
speed interface type device includes a DRAM unit for generating first clock  
and clock bar signals which do not have a phase difference from a main clock  
signal, and second clock and clock bar signals having 90° phase difference  
10 from the first clock and clock bar signals in a write operation, storing an  
inputted 4 bit data in one period of the main clock signal according to the first  
clock to second clock bar signals, synchronizing the stored data with data  
strobe signals according to the first clock to second clock bar signals in a read  
operation, and outputting a 4 bit data in one period of the main clock signal,  
15 and a controller for transmitting a command, address signal and data signal  
synchronized with the main clock signal to the DRAM unit in the write  
operation, and receiving data signals from the DRAM unit in the read  
operation.